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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,541	01/02/2002	Lawrence A. Clevenger	YOR9-2001-0508-US1	9395

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EXAMINER

LUK, LAWRENCE W

ART UNIT PAPER NUMBER

2187

DATE MAILED: 01/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/039,541		CLEVENGER ET AL.	
	Examiner		Art Unit	
	Lawrence W. Luk		2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 October 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The instant application having Application No. 10/039,541 has a total of 20 claims pending in the application; there are 6 independent claims and 14 dependent claims, all of which are rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bond et al. (5,724,728) in view of Levy (5,673,028).

Claim 1

As to claim 1, Bond et al. disclose in **figure 1B**, a system level device for battery and integrated circuit chip integrated circuit chip integration comprising: at least one battery **(28)**; at least one integrated circuit chip **(18)** powered by said at least one battery **(28)**; and a package **(12)** having a pair of opposed upright ends, said package **(12)** connected to any of said at least one battery **(28)** and said at least one integrated circuit chip **(18)**, wherein said at least one integrated circuit chip **(18)** lays on top of a portion of said package **(12)**, and wherein said at least one battery **(28)** overhangs said at least one integrated circuit chips **(18)**. (see column 3, lines 55-67 and column 4, lines 35-

46), except for Bond et al. fail to teach the limitation of wherein the battery is “solid state battery”.

Levy disclose in figure 4, the thin solid state battery on a chip. (**see column 6, lines 51-54**).

Bond et al. and Levy are analogous art because they are from same field of endeavor of the electric devices to be mounted on the circuit board include an integrated circuit and a battery cell.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to include solid state battery stacked on said package

The suggestion/motivation for doing so would have been to provides a particular solid state battery and constructions, which have enhanced power production capabilities as long as the life of the battery. (**see column 2, lines 17-20 of Levy**).

Therefore, it would have been obvious to combine Levy with Bond et al. for the solid state battery stacked on said package to obtain the invention as specified in claim 1.

Claim 2

As to claim 2, Bond et al. in view of Levy are applied supra, and further Bond et al. disclose in **figure 1B**, wherein said package (**12**) connects to said at least one integrated circuit chip (**18**) through an interior portion of said package (**12**). (**see column 4, lines 6-8**).

Claim 3

As to claim 3, Bond et al. in view of Levy are applied supra, and further Bond et al. disclose in **figure 1B**, wherein said at least one integrated circuit chip **(18)** connects to an upper indent portion of said package **(14)**; wherein said at least one battery **(solid state battery)** is larger than said at least one integrated circuit chip **(18)**. **(see column 4, lines 17-23)**

Claim 4

As to claim 4, Bond et al. in view of Levy are applied supra, and further Bond et al. disclose in **figure 1B**, wherein said at least one battery **(solid state battery)** connects to an underside of said package **(12)**. **(see column 4, lines 38-46)**

Claim 5

As to claim 5, Bond et al. in view of Levy are applied supra, and further Bond et al. disclose in **figure 1B**, a system level device for battery and integrated circuit chip integration comprising; at least one battery **(solid state battery)**; at least one integrated circuit chip **(18)** powered by said at least one battery **(solid state battery)**; and a package **(12)** connected to any of said at least one battery **(solid state battery)** and said at least one integrated circuit chip **(18)**, wherein said at least one battery **(solid state battery)** connects to a pair of opposed upright ends of said package **(12)**, wherein said at least one integrated circuit chip **(18)** is disposed between said at least one battery **(solid state battery)** and said package **(12)**, and wherein said at least one integrated circuit chip **(18)** lays on top of a portion of said package **(12)**. **(see column 3, lines 55-67 and column 4, lines 35-46).**

Claim 7

As to claim 7, Bond et al. in view of Levy are applied supra, and further Bond et al. disclose in **figure 1B**, a system level device for battery and integrated circuit chip integration comprising: a multi-chip module (**18, see column 3, lines 63-67**) integration system, wherein said multi-chip module integration system (**10**) comprises: a multi-chip module (**18 and 12**) having a pair of opposed upright ends; at least one battery (**solid state battery**) connected to said multi-chip module (**18 and 12**); and at least one integrated circuit chip (**18**) connected to said battery (**solid state battery**). wherein said integrated circuit chip (**18**) is powered by said battery (**solid state battery**), and wherein said at least one battery (**28**) overhang, and is larger than, said at least one integrated circuit chip (**18**), wherein said at least one integrate circuit chip (**18**) lays on top of a portion of said multi-chip module (**18 and 12**). (**see column 3, lines 55-67 and column 4, lines 35-46**).

Claim 8

As to claim 8, Bond et al. in view of Levy are applied supra, and further Bond et al. disclose in **figure 1B**, wherein said multi-chip module (**18 and 12**) connects to said at least one integrated circuit chip (**18**) through an interior portion of said multi-chip module (**18 and 12**). (**see column 3, lines 63-67**).

Claim 9

As to claim 9, Bond et al. in view of Levy are applied supra, and further Bond et al. disclose in **figure 1B, 4A, 4B**, wherein said at least one integrated circuit chip (**18**) connects (**20, 26a, 26b, 28, 32a, 32b**) to an upper indent portion of said multi-chip module (**18 and 12**). (**see column 3, lines 63-67**).

Claim 10

As to claim 10, Bond et al. in view of Levy are applied supra, and further Bond et al. disclose in **figure 1B**, a system level device for battery and integrated circuit chip integration comprising a multi-chip module integration system (**18, see column 3, lines 63-67**), wherein said multi-chip module integration system comprises: a multi-chip module (**18 and 12, see column 3, lines 60-62**); at least one battery (**solid state battery**) connected to said multi-chip module (**18 and 12**); and at least one integrated circuit chip (**18**) connected to said battery (**solid state battery**), wherein said integrated circuit chip (**18**) is powered by said battery (**28**), wherein said at least one battery (**solid state battery**) connects to a pair of opposed upright ends of said multi-chip module (**18 and 12**), wherein said at least one battery (**solid state battery**) overhangs, and is larger than, said at least one integrated circuit chip (**18**), and wherein said at least one integrated circuit chip (**18**) lays on top of a portion of said multi-chip module (**18 and 12**). (**see column 3, lines 55-67 and column 4, lines 35-46**).

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi (5,615,250) in view of Levy (5,673,028).

Claim 1

As to claim 1, Kobayashi disclose in **figure 3, 4**, a system level device for battery and integrated circuit chip integrated circuit chip integration comprising: at least one battery (**3**); at least one integrated circuit chip (**2**) powered by said at least one battery

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(3); and a package (20) having a pair of opposed upright ends (8, 9), said package (20) connected to any of said at least one battery (3) and said at least one integrated circuit chip (2), wherein said at least one integrated circuit chip (2) lays on top of a portion of said package (20), and wherein said at least one battery (3) overhangs said at least one integrated circuit chips (2). **(see column 3, line 40 to column 4, line 46)**, except for Kobayashi fail to teach the limitation of wherein the battery is "solid state battery".

Levy disclose in figure 4, the thin solid state battery on a chip. **(see column 6, lines 51-54)**.

Kobayashi and Levy are analogous art because they are from same field of endeavor of the electric devices to be mounted on the circuit board include an integrated circuit and a battery cell.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to include solid state battery stacked on said package

The suggestion/motivation for doing so would have been to provides a particular solid state battery and constructions, which have enhanced power production capabilities as long as the life of the battery. **(see column 2, lines 17-20 of Levy)**.

Therefore, it would have been obvious to combine Levy with Kobayashi for the solid state battery stacked on said package to obtain the invention as specified in claim 1.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyata (JP02001015673 A) in view of Levy (5,673,028).

Claim 11

As to claim 11, Miyata disclose in **figure 2**, an integrated chip structure comprising: an integrated circuit chip **(6)**; a battery **(8)** directly connected **(4)** to said integrated circuit chip **(6)** and a package **(1)** having a pair of opposed upright ends, said package **(1)** connected to any of said battery **(8)** and said integrated circuit chip **(6)**, wherein said integrated circuit chip **(6)** lays on top of a portion of said package **(1)**, and wherein said at least one battery **(8)** overhangs said at least one integrated circuit chip **(6)** **(see Abstract)**, except for Miyata fail to teach the limitation of wherein the battery is “solid state battery” and wherein an upper surface of said pair of opposed upright ends is planar with an upper surface of said integrated circuit chip.

In regards to the planar upper surface, it would have been obvious to one skilled in the art to modify the upright ends of Miyata to planar with the integrated chip, Miyata already teaches raised ends near location **(5)** where the elements **(2)** meets the substrate **(1)**. Thereby, it would be merely a shift in location of parts when operation of device is not otherwise modified, In Japikse, 86 USPQ 70 (CCPA 1950).

Levy disclose in figure 4, the thin solid state battery on a chip. **(see column 6, lines 51-54)**.

Miyata and Levy are analogous art because they are from same field of endeavor of the electric devices to be mounted on the circuit board include an integrated circuit and a battery cell.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to include solid state battery stacked on said package

The suggestion/motivation for doing so would have been to provides a particular solid state battery and constructions, which have enhanced power production capabilities as long as the life of the battery. **(see column 2, lines 17-20 of Levy).**

Therefore, it would have been obvious to combine Levy with Miyata for the solid state battery stacked on said package to obtain the invention as specified in claim 11.

6. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuura (6,673,484) in view of Levy (5,673,028).

Claim 16

As to claim 16, Matsuura disclose in **figure 2A, 2B**, an integrated chip structure comprising: a package **(20)** having a pair of opposed upright ends; an integrated circuit chip **(12)** mounted on said package **(20)**; a battery **(40)** directly connected to said package **(20, see column 4, lines 30-46)** and electrically connected to said integrated circuit chip **(12)**, wherein said integrated circuit chip **(12)** lays on top of a portion or said package **(20)**, and wherein said at least one battery **(40)** overhangs said at least one integrated circuit chip **(12)**. **(see column 4, lines 16-46)**, except for Miyata fail to teach the limitation of wherein the battery is "solid state battery".

Levy disclose in figure 4, the thin solid state battery on a chip. **(see column 6, lines 51-54).**

Matsuura and Levy are analogous art because they are from same field of endeavor of the electric devices to be mounted on the circuit board include an integrated circuit and a battery cell.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to include solid state battery stacked on said package

The suggestion/motivation for doing so would have been to provides a particular solid state battery and constructions, which have enhanced power production capabilities as long as the life of the battery. **(see column 2, lines 17-20 of Levy).**

Therefore, it would have been obvious to combine Levy with Matsuura for the solid state battery stacked on said package to obtain the invention as specified in claim 16.

Claim 17

As to claim 17, Matsuura in view of Levy are applied supra, and further Matsuura disclose in **figure 2A, 2B**, wherein said battery **(40)** is held adjacent to said integrated circuit chip **(12)** by said package **(20)**. **(see column 4, lines 29-46)**

Claim 18

As to claim 18, Matsuura in view of Levy are applied supra, and further Matsuura disclose in **figure 4A**, wherein said package **(20)** is between said battery **(40)** and said integrated circuit chip **(12)**. **(see column 6, lines 16-32)**

Claim 19

As to claim 19, Matsuura in view of Levy are applied supra, and further Matsuura disclose in **figure 4A**, wherein said battery **(40)** is electrically connected to said integrated circuit chip **(12)** through said package **(20)**. **(see column 6, lines 28-32)**

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuura (6,673,484) in view of Levy (5,673,028) as applied to claim 16 above, and further in view of Tuttle (6,548,207).

Claim 20

As to claim 20, Matsuura in view of Levy disclose the elements as claimed except Matsuura in view of Levy fails to teach the limitation of **wherein said solid state battery comprises multiple solid state batteries stacked on said package**.

Tuttle disclose in figure 2 and 8, wherein said (solid state) battery comprises multiple (solid state) batteries **(32, 28)** stacked on said package **(16)**. **(see column 1, lines 60-61, column 4, lines 15-16)**.

Matsuura, Levy and Tuttle are analogous art because they are from same field of endeavor of the electric devices to be mounted on the circuit board include an integrated circuit and a battery cell.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to include multiple batteries stacked on said package

The suggestion/motivation for doing so would have been to provides a particular button-type battery circuits and constructions, which have enhanced power production capabilities and/or battery lifetimes. **(see column 1, lines 32-37 of Tuttle)**.

Therefore, it would have been obvious to combine Tuttle with Matsuura and Levy for the multiple batteries stacked on said package to obtain the invention as specified in claim 20.

8. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyata (JP02001015673A) in view of Levy (5,673,028) as applied to claim 11 above, and further in view of Levy (4,026,304).

Claims 12 and 13

As to claims 12 and 13, Miyata disclose the elements as claimed except Miyata fails to teach the limitation of **further comprising solder connections between said battery and said integrated circuit chip.**

Levy disclose in figure 1 and 2, further comprising solder connections between said battery and said integrated circuit chip. **(see column 6, lines 6-10).**

Miyata and Levy are analogous art because they are from same field of endeavor of the electric devices to be mounted on the circuit board including an integrated circuit and a battery cell.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to include solder connections between said battery and said integrated circuit chip.

The suggestion/motivation for doing so would have been to provides a construction process using conventional soldering techniques **(see column 6, lines 8-10 of Levy).**

Therefore, it would have been obvious to combine Levy with Miyata for forming the electrical connection between the battery and the integrated circuit chip as specified in claim 12-13.

Claim 14

As to claim 14, Miyata in view of Levy are applied supra, and Miyata further disclose in **figure 2**, said wherein said package **(1)** surrounds said battery **(8)** and said integrated circuit chip **(6)**.

Claim 15

As to claim 15, Miyata in view of Levy are applied supra, and Miyata further disclose in figure 2, said battery **(8)** is directly connected **(5)** to said package **(20)**. **(see Figure 2 and Abstract)**.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bond et al. (5,724,728) in view of Tuttle (6,548,207).

Claim 6

As to claim 6, Bond et al. disclose the elements as claim 3, except Bond et al. fails to teach the limitation of **a stack of connected batteries**.

Tuttle disclose in figure 2 and 8, wherein said battery comprises a stack of connected batteries **(32, 28)**. **(see column 1, lines 60-61, column 4, lines 15-16)**.

Bond et al. and Tuttle are analogous art because they are from same field of endeavor of the electric devices to be mounted on the circuit board to include an integrated circuit and a battery cell.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a stack of connected batteries.

The suggestion/motivation for doing so would have been to provides a particular button-type battery circuits and constructions, which have enhanced power production capabilities and/or battery lifetimes. **(see column 1, lines 32-37 of Tuttle).**

Therefore, it would have been obvious to combine Tuttle with Bond et al. for a stack of connected batteries to obtain the invention as specified in claim 20.

10. **RELEVANT ART CITED BY THE EXAMINER**

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure.

See **MPEP 707.05 (c)**.

The following references teach **the electric devices to be mounted on the circuit board include an integrated circuit and a battery cell.**

<u>US PATENT NUMBER</u>	<u>FIGURES</u>
6,906,407	2-4
6,459,593	2
5,963,429	3

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5,498,903 1, 3-5

4,381,458 1, 3

FOREIGN PATENT NUMBERFIGURES

FR 2822572 1-3

DE 19612718 1, 3, 4

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence W Luk whose telephone number is (571) 272-2080. The examiner can normally be reached on 7 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding are (703) 746-7239, (571) 272-2100 for regular communication and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to receptionist whose telephone number is (571) 272-2100.

LWL

December 27, 2005

Lawrence Luk
examiner
12/27/2005